AMD Athlon™ 64 FX Processor Product Data Sheet

- **Compatible with Existing 32-Bit Code Base**
  - Including support for SSE, SSE2, SSE3*, MMX™, 3DNow!™ technology and legacy x86 instructions
    *SSE3 supported by Rev. E and later processors
  - Runs existing operating systems and drivers
  - Local APIC on-chip
- **AMD64 Technology**
  - AMD64 technology instruction set extensions
  - 64-bit integer registers, 48-bit virtual addresses, 40-bit physical addresses
  - Eight additional 64-bit integer registers (16 total)
  - Eight additional 128-bit SSE/SSE2/SSE3 registers (16 total)
- **Multi-Core Architecture**
  - Single-core or dual-core options
  - Discrete L1 and L2 cache structures for each core
- **64-Kbyte 2-Way Associative ECC-Protected L1 Data Cache**
  - Two 64-bit operations per cycle, 3-cycle latency
- **64-Kbyte 2-Way Associative Parity-Protected L1 Instruction Cache**
  - With advanced branch prediction
- **16-Way Associative ECC-Protected L2 Cache**
  - Exclusive cache architecture—storage in addition to L1 caches
  - Up to 1 Mbyte per L2 cache
- **Machine Check Architecture**
  - Includes hardware scrubbing of major ECC-protected arrays
- **Power Management**
  - Multiple low-power states
  - System Management Mode (SMM)
  - ACPI compliant, including support for processor performance states in some models

940-Pin Package Specific Features

- **Refer to the *AMD Functional Data Sheet, 940-Pin Package, order# 31412*, for functional, electrical, and mechanical details of 940-pin package processors.**
- **Packaging**
  - 940-pin lidded ceramic micro PGA
  - 1.27-mm pin pitch
  - 31x31-row pin array
  - 40mm x 40mm ceramic substrate
  - Ceramic C4 die attach
- **Integrated Memory Controller**
  - Low-latency, high-bandwidth
  - 144-bit DDR SDRAM at 100, 133, 166, and 200 MHz
  - Supports up to eight registered DIMMs
  - ECC checking with double-bit detect and single-bit correct
- **Electrical Interfaces**
  - HyperTransport™ technology: LVDS-like differential, unidirectional
  - DDR SDRAM: SSTL_2 per JEDEC specification
  - Clock, reset, and test signals also use DDR SDRAM-like electrical specifications.
- **HyperTransport™ Technology to I/O Devices**
  - One 16-bit link supporting speeds up to 800 MHz (1600 MT/s) or 3.2 Gigabytes/s in each direction

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939-Pin Package Specific Features

- **Refer to the *AMD Functional Data Sheet, 939-Pin Package, order# 31411*, for functional, electrical, and mechanical details of 939-pin package processors.**
- **Packaging**
  - 939-pin lidded micro PGA
  - 1.27-mm pin pitch
  - 31x31-row pin array
  - 40mm x 40mm organic substrate
  - Organic C4 die attach
- **Integrated Memory Controller**
  - Low-latency, high-bandwidth
  - 144-bit DDR SDRAM at 100, 133, 166, and 200 MHz
  - Supports up to four unbuffered DIMMs
  - ECC checking with double-bit detect and single-bit correct
- **Electrical Interfaces**
  - HyperTransport™ technology: LVDS-like differential, unidirectional
  - DDR SDRAM: SSTL_2 per JEDEC specification
  - Clock, reset, and test signals also use DDR SDRAM-like electrical specifications
- **HyperTransport™ Technology to I/O Devices**
  - One 16-bit link supporting speeds up to 1 GHz (2000 MT/s) or 4 Gigabytes/s in each direction

Socket AM2 Processor Specific Features

- **Refer to the *Socket AM2 Processor Functional Data Sheet, order# 31117*, for functional and mechanical details of socket AM2 processors.**
- **Refer to the *AMD NPT Family 0Fh Processor Electrical Data Sheet, order# 31119*, for electrical details of socket AM2 processors.**
- **Packaging**
  - Lidded micro PGA
  - 1.27-mm pin pitch
  - 31x31 grid array
  - Compliant with RoHS (EU Directive 2002/95/EC) with lead used only in small amounts in specifically exempted applications
- **Integrated Memory Controller**
  - Low-latency, high-bandwidth
  - 144-bit DDR2 SDRAM controller operating at up to 400 MHz
  - Supports up to four unbuffered DIMMs
  - ECC checking with double-bit detect and single-bit correct
- **Electrical Interfaces**
  - HyperTransport™ technology: LVDS-like differential, unidirectional
  - DDR2 SDRAM: SSTL_1.8 per JEDEC specification
  - Clock, reset, and test signals also use DDR2 SDRAM-like electrical specifications
- **HyperTransport™ Technology to I/O Devices**
  - One 16-bit link supporting speeds up to 1 GHz (2000 MT/s) or 4 Gigabytes/s in each direction

Fr3 (1207) Processor Specific Features

- **Refer to the *Fr3 (1207) Processor Functional Data Sheet*, order# 41696 for functional and mechanical details of Fr3 (1207) processors.**
- **Refer to the *AMD NPT 0Fh Family Processor Electrical Data Sheet*, order# 31119 for electrical details of Fr3 (1207) processors.**
- **Intended for use in pairs on a platform.**
- **Electrical Interfaces**
  - HyperTransport™ technology: LVDS-like differential, unidirectional
  - DDR2 SDRAM: SSTL_1.8 per JEDEC specification
  - Clock, reset, and test signals also use DDR2 SDRAM-like electrical specifications
- **Packaging**
  - Lidded Land Grid Array package
  - 35 x 35 grid array
  - Compliant with RoHS (EU Directive 2002/95/EC) with lead used only in small amounts in specifically exempted applications
- **Integrated Memory Controller**
  - Low-latency, high-bandwidth
  - 144-bit DDR2 SDRAM at up to 400 MHz
  - Supports up to two unbuffered DIMMs
- **HyperTransport™ Technology to I/O Devices**
  - Three links, 16-bits in each direction, each supports up to 2000 MT/s or 4.0 GB/s in each direction
  - Each link supports connections to I/O devices, and any one of the three available links may connect to another AMD Athlon™ 64 FX Fr3 (1207) processor.

Revision History

Date	Revision	Description
May 2007	3.16	Sixth public release. Added Fr3 (1207) processor specific features.
September 2006	3.14	Fifth public release. Removed change bars.
August 2006	3.12	Added RoHS compliance statement. Added asterisk note to SSE3.
June 2006	3.08	Fourth public release. Added socket AM2 processor specific features and SSE3 support. Added revision history.
June 2004	3.05	Third public release. Changed to 2-page format. Added 940-pin and 939-pin package specific features.
February 2004	3.03	Second public release. Multiple changes to the eight chapters.
September 2003	3.00	Initial public release.